NATIONAL WORKSHOP ON MODELS OF EMBEDDED COMPUTATION

A model of computation (MoC) is an abstraction of a real computing device. MoC's have been evolving during the history of computing. The Turing Machine is a prominent example of computational model developed to investigate the question "what is computable?" Later the focus changed to the question "what can be computed in reasonable time and with reasonable resources?" which spun off the theories of algorithmic complexity and the notion of asymptotic complexity. The complexity theories rest on the assumption that one kind of computational model or machine abstraction can simulate another one with a bounded well defined overhead.

The present workshop is proposed to expose the participants to different models of computation, relation between sequential and parallel machines, untimed asynchronous and timed MoCs, MoC framework and interfaces etc. with special emphasis to MoC for embedded systems. Embedded systems with heterogeneous architectures leading to SoC (System on Chip) are the need of the day and the workshop is intended to cover the existing formalisms such as Finite State Machines (FSM, FSMD), Program state Machines (PSM), Synch ronous/reactive models, Discrete event system models. Models of embedded computation are very important and significant topic as to use the "right" computational model for a particular design task can greatly facilitate the design process and quality of the result.

From an MoC perspective, several important issues are open research topics and will be addressed during the workshop such as effective integration of different MoC's in terms of global optimization and synthesis. Topics to be covered are:

- Notion of Computability
- Models of Computations : Turing Machines, Lambda Calculus, Partial Recursive Functions, Register Machines and Markov Algorithms.
- Algorithmic Complexity
- Invariance Thesis and parallel computation Thesis
- Models of sequential and Parallel Computation
- Real Time Systems
- Heterogeneity
- MoC Framework (FSM, HCFSM, PSM, Code sign FSM, Message Sequence Charts Petrinets) : Process and Signals, Untimed MoCs, Synchronous MoCs, Discrete Time MoCs.

The workshop is intended for young faculty and researchers from Computer Science, Mathematics and Electronics interested in the field.

Eminent National experts from both "Theory of Computation" and "Design of Embedded systems" have been invited to be resource persons in the worshop. Those who have confirmed are:

1. Prof. Aditya Shastri, Banasthali Vidyapith	_	Theory of Computation
2. Dr. A.S. Mandal, CEERI Pilani	-	Shared state FSM and functionality driven
3. Dr. C.P. Ravikumar, Texas Instruments, Bangalore	-	automata partitioning Tutorials on Embedded Computing on System-on- Chip
4. Dr. Kamal Lodaya, IIMSc, Chennai	-	Finite Automata &
5. Prof. Naresh Jotwani, DA-IICT, Gandhi Nagar	-	Embedded Computation FSM & Regular languages, Classes P and NP, Turing
6. Prof. R. Ramanujam, IIMSc, Chennai	-	Machines Automate Models with concurrency and
7. Prof. Rekha Govil, Banasthali Vidyapith	-	Real Time issues in embedded. Computing
8. Dr. S. C. Bose, CEERI Pilani	-	Text to Speech - an
9. Dr. Vineet Sahula, MNIT Jaipur	-	architectural exploration Models of Computation: Application to Embedded Hardware

ADVISORY COMMITTEE

Prof. Aditya Shastri Director, Banasthali Vidyapith

Prof. B. D. Acharya DST, Govt. of India, New Delhi

Dr. C.P. Ravikumar Texas Instruments, Bangalore

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